Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (current amended). A circuit configuration for use in testing a semiconductor memory, comprising:

an output register for receiving digital data;

a plurality of shift registers for serially outputting the digital data to be received by the output register, wherein each of the plurality of shift registers includes a feedback path for enabling the digital data output by each individual register of the plurality of shift registers to be input back into the same individual register in a same sequence as the digital data is output from the same individual register; and

means for selecting one of the plurality of shift registers for outputting digital data to the output register.

Claim 2 (original). The circuit configuration of claim 1, wherein each one of the plurality of shift registers has a different bit storage capacity.

Claim 3 (original). The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 48-bit register.

Claim 4 (original). The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 33-bit register.

Claim 5 (original). The circuit configuration of claim 1, wherein one of the plurality of shift registers is a 20-bit register.

Claim 6 (original). The circuit configuration of claim 1, wherein the output register has a bit storage capacity equal to a bit storage capacity of a largest one of the plurality of shift registers.

Claim 7 (original). The circuit configuration of claim 1, further comprising an output pin which is strobed to examine contents of the output register.

Claim 8 (previously presented). The circuit configuration of claim 1, wherein the means for selecting comprises a multiplexer interposed between the output register and the plurality of shift registers.

Claim 9 (original). The circuit configuration of claim 1, wherein the semiconductor, memory is a built-in self repair (BISR) memory.

Claim 10 (original). The circuit configuration of claim 1, wherein the digital data, received by the output register is divided into patterns corresponding to the plurality of shift registers.

Claim 11 (Currently amended). A method for use in testing a semiconductor memory, comprising steps of:

serially outputting digital data from a shift register into an output register;

inputting the digital data back into the shift register in a same sequence as the digital data is output from the shift register; and

examining the digital data in the output register.

Claim 12 (original). The method of claim 11, wherein the shift register is disabled while the digital data in the output register is examined.

Claim 13 (original). The method of claim 11, wherein the semiconductor memory is a built-in self repair (BISR) memory.

Claim 14 (previously presented). The method of claim 11 further comprising the step of determining whether any bit errors are present.

Claim 15 (previously presented). The method of claim 11 further comprising the step of determining whether output from an additional register is to be output into the output register.

Claim 16 (previously presented). The circuit configuration of claim 1, wherein the semiconductor memory is a plurality of built-in self repair (BISR) memory and each of the plurality of shift registers is connected to one of the plurality of BISR memory.